Total Dose Test Report for Micron and Hynix 4G NAND Flash Nonvolatile Memory

Timothy R. Oldham[1] and Mark Friendlich[2]
1. QSS Group, Inc., Seabrook, MD 20706
2. Muniz Engineering, Inc., Seabrook, MD 20706

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I. Introduction

The purpose of this test was to determine the susceptibility to total ionizing radiation dose (TID) of the Micron and Hynix 4G NAND flash nonvolatile memories. This test was supported by the NASA Electronics Parts and Packaging (NEPP) Program.

II. Devices Tested

These NAND Flash memories are non-volatile memories that use a floating gate NAND cell, and a serial organization. They also provide a standard interface for pin and function drop-in compatibility. We believe these parts were burned-in before leaving the factory, so it is not possible to do a controlled experiment to look at burn-in effects. In any case, there is no plan to do our own burn-in. Detailed device information is provided in Table I. The parts have 4K blocks, up to 80 of which can be "bad," as identified by the manufacturer. The blocks are 128Kx8, with 64 pages, 2Kx8. In this case, eight samples were irradiated, four from each manufacturer, all of which had some bad blocks. There was also one unirradiated control device from each manufacturer. The parts have a nominal 3.3 V power supply (range is 2.7-3.6 V), plus an internal charge pump to generate higher voltages for writing and erasing.

Generic Part Number:	
Full Part Number	HY27UF084G2M
Manufacturer:	Hynix
Lot Date Code (LDC):	636A
Quantity Tested:	5
Serial Numbers of Control Sample:	1
Serial Numbers of Radiation Samples:	2, 3, 4, 5,
Part Function:	NAND Flash Memory

Part Technology:	CMOS
Case Markings:	Hynix KOR HY27UF084G2M TPCB 636A
Package Style:	48 pin TSOP
Test Equipment:	Power Supply (+3.3V) Digital test board. Multimeters
Test Engineer:	M. Friendlich
Dose Levels (krad (Si)):	10, 15, 20, 30, 40, 50, 60, 75, and 100krads(Si) continuing in 50krads (Si) steps until functional failure.
Target dose rate (rad (Si)/min):	1200-1800

Generic Part Number:	
Full Part Number	MT29F4G08AAAWP
Manufacturer:	Micron
Lot Date Code (LDC):	0628
Quantity Tested:	5
Serial Numbers of Control Sample:	1
Serial Numbers of Radiation Samples:	2, 3, 4, 5,
Part Function:	NAND Flash Memory
Part Technology:	CMOS

Case Markings:	0628 I-I MT 29F4G08AAA WP A
Package Style:	48 pin TSOP
Test Equipment:	Power Supply (+3.3V) Digital test board. Multimeters
Test Engineer:	M. Friendlich
Dose Levels (krad (Si)):	10, 15, 20, 30, 40, 50, 60, 75, and 100krads(Si) continuing in 50krads (Si) steps until functional failure.
Target dose rate (rad (Si)/min):	1200-1800

III. Test Facility

Testing was at the Co-60 facility at GSFC, which is a room air source, where the pencils are raised up out of the floor, during exposures. Active dosimetry is performed, using air ionization probes. Testing is done in a step/stress manner, using a standard Pb/Al filter box. Dose rate typically varies slightly from one exposure to the next, up to 30 rads/s. Most exposures are near the maximum dose rate, as required by MIL-STD Test Method 1019.6. Time intervals for testing between exposures are also within the limits stated in 1019.6 (one hour after exposure to start electrical characterization, two hours to begin the next exposure). Parts were under DC bias during exposures, but not actively exercised.

IV. Test Procedure

The test devices were programmed with a checkerboard pattern (AA) during exposures, and biased at 3.6 V (3.3 V nominal power supply, plus 10%), but the devices were not actively exercised during exposures. Four parts, two from each manufacturer, were read (only) between exposures, to look for problems related to the integrity of the individual bits. The other four parts were exercised between exposures—read, erased, and written into four different patterns. The patterns were checkerboard (AA), checkerboard complement (55), all ones, and all zeroes. In each of these tests, the entire memory is read, or erased, or programmed in one operation, with the commands entered manually. There is also a dynamic test mode, where each block is read, erased, and programmed,

then the next block, and so on until the entire memory is completed. A block diagram of the test apparatus is shown in Fig. 1.

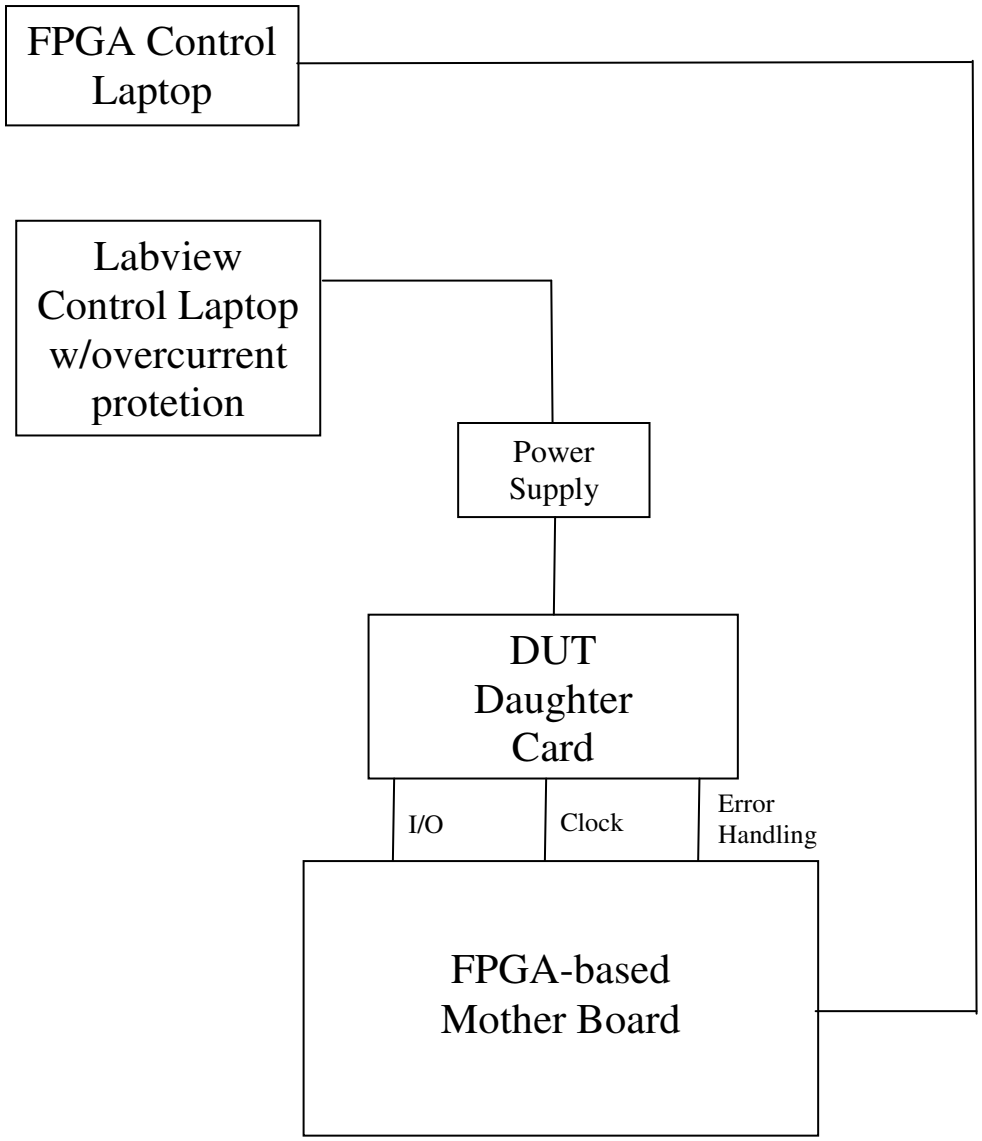

Fig. 1. Block diagram of the flash memory test apparatus.

V. Results

DUTs 1,2,5, and 6 were tested in read-only mode, while DUTs 3,4,7, and 8 were exercised in all the test patterns and the dynamic mode, as described above. DUTs 1-4 were Hynix parts, while DUTs 5-8 were from Micron. All the DUTs had some bad blocks, before irradiation. At the 10, 20, and 30 krad (SiO_2) exposure levels, there were no errors in any device, in any test mode, except those identified in the bad blocks prior to irradiation, with one exception. At the 30 krad level, DUT 2 (Hynix read only) had three or four bad bits in multiple reads, both with and without cache. These bits were not reset immediately, but were left undisturbed for the next exposure increment. At the next

data point, 50 krad (SiO_2), DUT 2 had 13,700 bad bits initially. This number was reduced by 100-200 in each subsequent re-reading, indicating some annealing. There was no difference between cache and non-cache mode, except that the cache measurements were done after the non-cache reads, which allowed more time for annealing. This DUT was then reset successfully, and the exposure was continued. However DUT 4 (Hynix, fully exercised) lost the ability to program consistently. It was judged to have failed, and was removed from the test. It could erase a pattern successfully, to FF, but the next programming step resulted in several tens of thousands of errors, to hundreds of thousands of errors. The exact number varied with the pattern, but the errors appeared to be incomplete writes, randomly distributed. Also at the 50 krad point, DUT 5 (Micron, read only) had one block that failed, apparently in all test modes. Since the rest of the circuit appeared to be fully functional, the test was continued with one (additional) bad block. At the 75 krad (SiO_2) data point, the remaining Hynix parts failed. The read only parts each had a few hundred thousand errors, which needed to be reset. But the erase and write operations were not successful on any of the DUTs. The Micron parts were still functional at this level, but they had isolated block failures. These blocks could be written to zeroes successfully, but not erased to ones. The two read-only devices had errors in the initial read operation, which appeared to be two bad blocks on DUT 5, and four bad blocks on DUT 6. These DUTs could be reset, except for the bad blocks. DUT 7 had one bad block, and DUT 8 had two bad blocks. At the 100 krad (SiO_2), the two Micron read-only parts had two bad blocks, each, but they appeared otherwise, to be fully functional. DUT 7 had one bad block, in all test modes, but it was otherwise fully functional. DUT 8 failed, the first Micron part to do so. In the cache-read mode, there was a watchdog error—an indication of chip not ready. In the non-cache mode, one of the two previously bad blocks seemed to have repaired itself, but there were a few tens of thousands of other errors, randomly distributed. These could not be erased or programmed, so the DUT was considered to have failed. It was removed from the test. At 150 krad (SiO_2), the read only devices, DUTs 5 and 6, had about 396,000 and 106,000 errors, respectively, in the initial read. Of these, about 105,000 could not be reset, so the parts were considered to have failed, and they were removed from the test. DUT 7 also had about 522,000 errors in the initial read, but most of these were successfully reset. The part appeared to be fully functional, except that one or two blocks (depending on the test) appeared to be bad. These could have been screened out, and the test continued. However, this was not done, because it would not have been useful for only one part.